M62213P/FP

General Purpose High Speed PWM Control IC

REJ03D0838-0300
Rev.3.00
Sep 05, 2007

Description

M62213P/FP is designed as a general purpose high-speed PWM control IC.

This small 10 pin package contains many function and protection circuits allowing simpler peripheral circuits and compact set design.

This IC can operate high speed switching (700 kHz Max.) with high speed PWM comparator and current limiting circuit.

Features

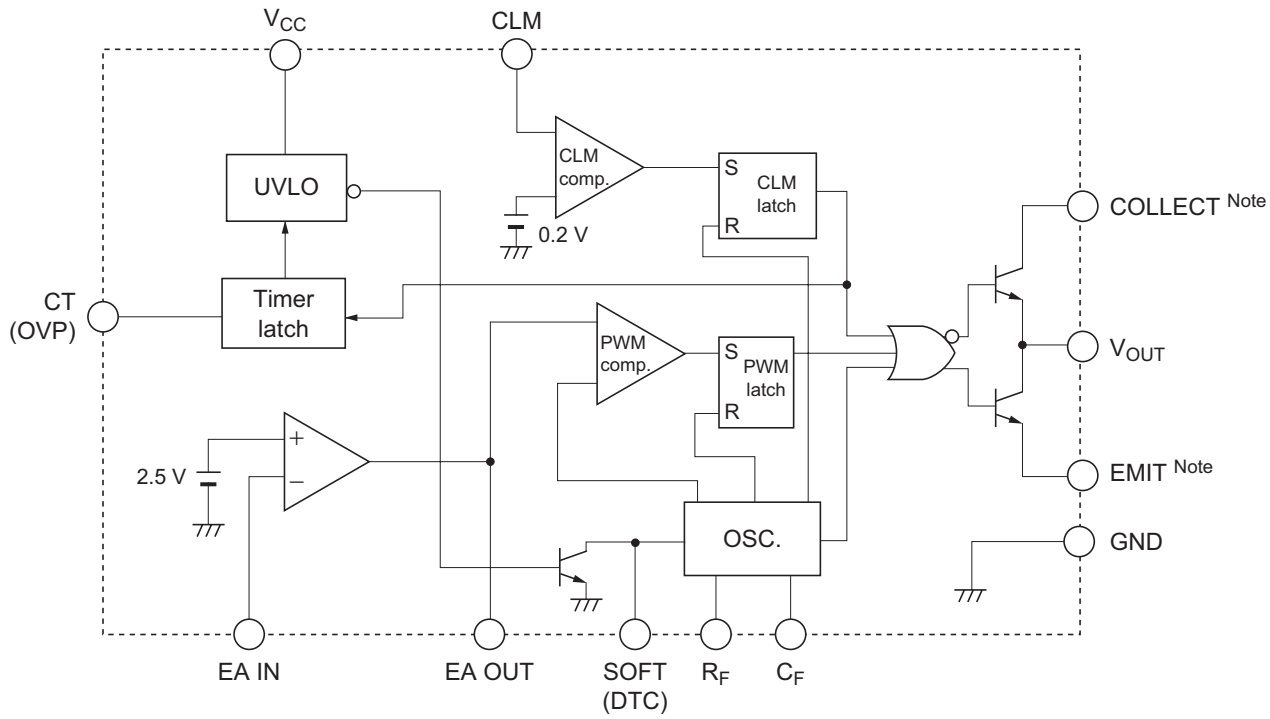
- 700 kHz operation to MOS FET
  - Output current $I_O = \pm 1$ A
  - Totempole output
- Timer type latch protection circuit with OVP
- Soft start operation is possible (with dead time control)
- Built-in OP Amp for feedback control (photo coupler can be driven)
- High speed pulse-by-pulse current limiting
- Small size 10-pin SOP package

Application

Switching Regulator

DC/DC Converter

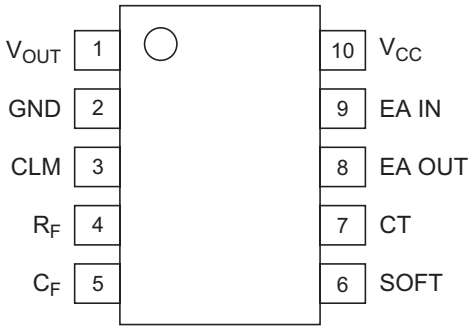
Block Diagram



Note: GND terminal is connected to emitter terminal as M62213FP in IC inside.
And V_{CC} terminal is connected to collector terminal as M62213FP in IC inside.

Pin Arrangement

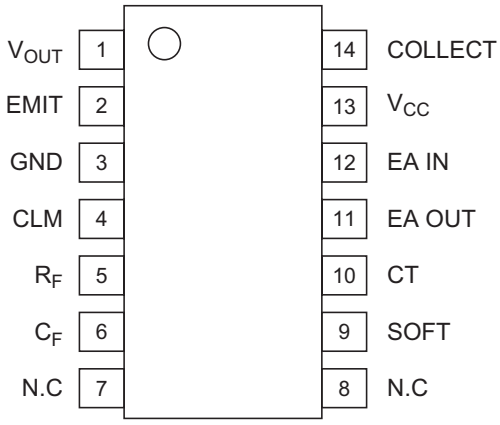
M62213FP



(Top view)

Outline: PRSP0010DB-A (10P2N-A)

M62213P



(Top view)

Outline: PRDP0014AA-A (14P4)

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Condition	
Supply voltage	V_{CC}	36	V		
Output terminal current	I_{OUT}	150	mA		Continuous
		1.0	A		Peak
CT terminal supply voltage	V_{CT}	36	V		
EA IN terminal supply voltage	$V_{EA\ IN}$	10	V		
CLM terminal supply voltage	V_{CLM}	–0.3 to +4.0	V		
Power dissipation	Pd	1500	mW		P
		440			FP
Thermal derating	Kθ	12	mW/°C	Ta ≥ 25°C	P
		3.52			FP
Operating temperature	Topr	–20 to +85	°C		
Storage temperature	Tstg	–40 to +150	°C		

Electrical Characteristics

(Ta = 25°C, V_{CC} = 14 V, unless otherwise noted.)

Block	Item	Symbol	Limits			Unit	Test Conditions
			Min.	Typ.	Max.		
All device	Supply voltage range	V_{CC}	$V_{CC(STOP)}$	—	35	V	
	Operation start-up voltage	$V_{CC(START)}$	11.5	12.5	13.5	V	
	Operation stop voltage	$V_{CC(STOP)}$	7.6	8.3	9.0	V	
	Start-up and stop voltage difference	ΔV_{CC}	3.5	4.2	5.1	V	
	Stand-by current	I_{CCL}	90	180	270	µA	$V_{CC} = V_{CC(START)} - 0.5V$
	Operating current	I_{CCO}	7.5	13	22	mA	
	Timer latch circuit current	I_{CCOFF}	0.9	2.0	3.0	mA	V_{CC} = 14V
			0.8	1.8	2.7	mA	$V_{CC} = V_{CC(STOP)} + 0.2V$
CT	CT term. “H” threshold voltage	V_{THCTH}	3.5	4.0	4.5	V	
	CT term. “L” threshold voltage	V_{THCTL}	0.4	0.7	1.0	V	
	CT term. discharge current	I_{CTDCHG}	70	100	130	µA	In normal operation
	CT term. charge current	I_{CTCHG}	–33	–15	–5	µA	In CLM actuating
Error Amp	Reference voltage	V_B	2.4	2.5	2.6	V	
	Input bias current	I_B	–300	–100	0	nA	
	Open loop gain	A_V	—	70	—	dB	
	Unity gain bandwidth	f_T	—	1	—	MHz	
	Output source current	I_{OS}	–140	–100	–60	µA	When $V_{EA\ IN}$ = 0V
	Output voltage (High)	V_{Om+}	4.7	5.25	6.25	V	
	Output voltage (Low)	V_{Om-}	0	0.1	0.3	V	
CLM	CLM term. threshold voltage	V_{THCLM}	180	200	220	V	
	CLM term. output current	I_{OUTCLM}	–270	–200	–140	µA	V_{CLM} = 0V
	CLM term. delay time	T_{PDCLM}	—	90	—	ns	Delay time to output
SOFT	Input voltage range at 0% duty	$V_{SOFT\ (0\%)}$	0	—	0.5	V	Soft term. voltage range to set 0% duty
	Input. voltage at 50% duty	$V_{SOFT\ (50\%)}$	—	2.7	—	V	Soft term. voltage at 50% duty
	Maximum duty	Duty Max	80	90	99	%	
	Soft term. input current	I_{SOFT}	–65	–50	–31	µA	
OSC	Maximum oscillation frequency	f_{OSCmax}	—	—	700	kHz	
	Oscillation frequency	f_{OSC}	150	200	250	kHz	CF = 270pF, RF = 69kΩ
Output	Output low voltage	V_{OL1}	—	0.04	0.4	V	V_{CC} = 14V, I_O = 10mA
		V_{OL2}	—	0.3	1.4	V	V_{CC} = 14V, I_O = 100mA
	Output high voltage	V_{OH1}	12.0	12.7	—	V	V_{CC} = 14V, I_O = –10mA
		V_{OH2}	11.5	12.5	—	V	V_{CC} = 14V, I_O = –100mA
	Output voltage rise time	T_{RISE}	—	50	—	ns	No load
	Output voltage fall time	T_{FALL}	—	35	—	ns	No load

Function Description And Application

EA IN, EA OUT Terminal

Circuit for EA OUT terminal is connected to constant current load (100 μA Typ.) shown in figure 1. Output voltage of error amp. is controlled by the output transistor to provide current-sense comp. with the controlled voltage.

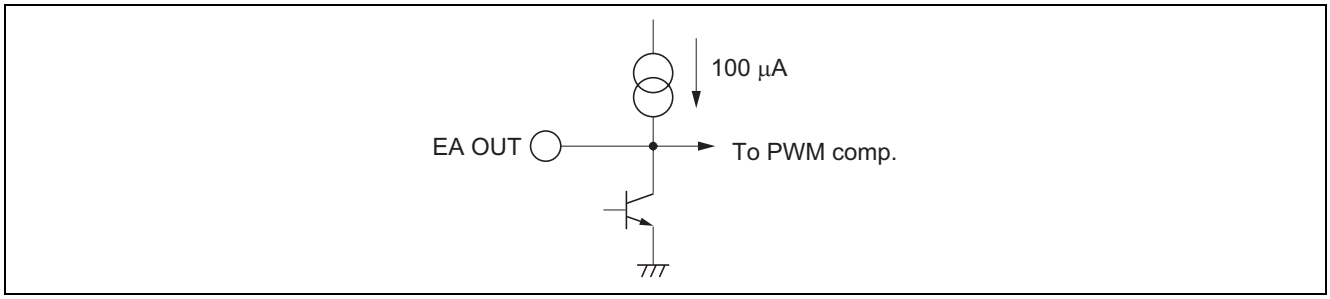


Figure 1 Circuit Diagram of EA OUT Terminal

1. Peripheral circuit of error amp
   Detected voltage divided by R1 and R2 is input to EA IN terminal in such case as fly-back system where V_{CC} line voltage is proportional to output voltage, or in the case that the voltage detection is made on the primary side. In this case operating region is set by R1 and R2, and AC gain by R1 // R2, RF.

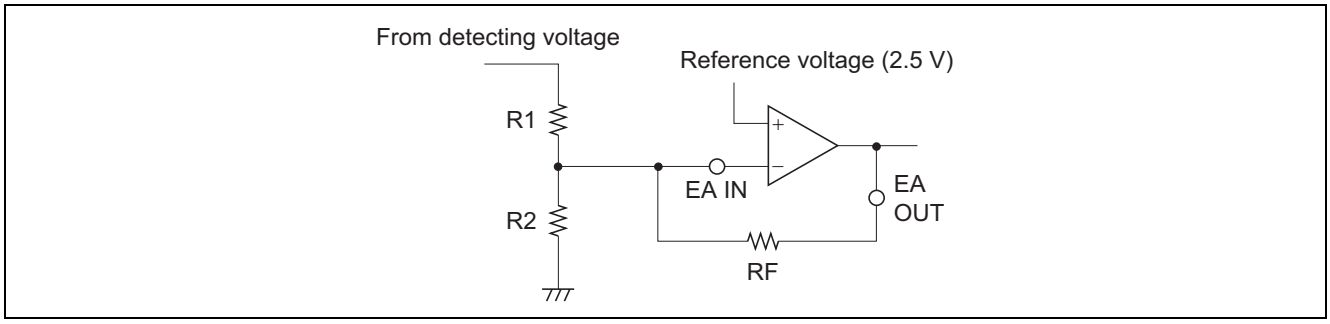


Figure 2 Method to Detect The Voltage on The Primary Side

In the case that feed forward system by photo-coupler is applied, following two methods are available.
One is the method by error amp. as in figure 3-1, the other is by the direct connection to photo-coupler as in figure 3-2.
When photo-coupler is directly connected to EA OUT terminal, input terminal of error amp. is connected to GND, photo-coupler is connected directly to EA OUT terminal.

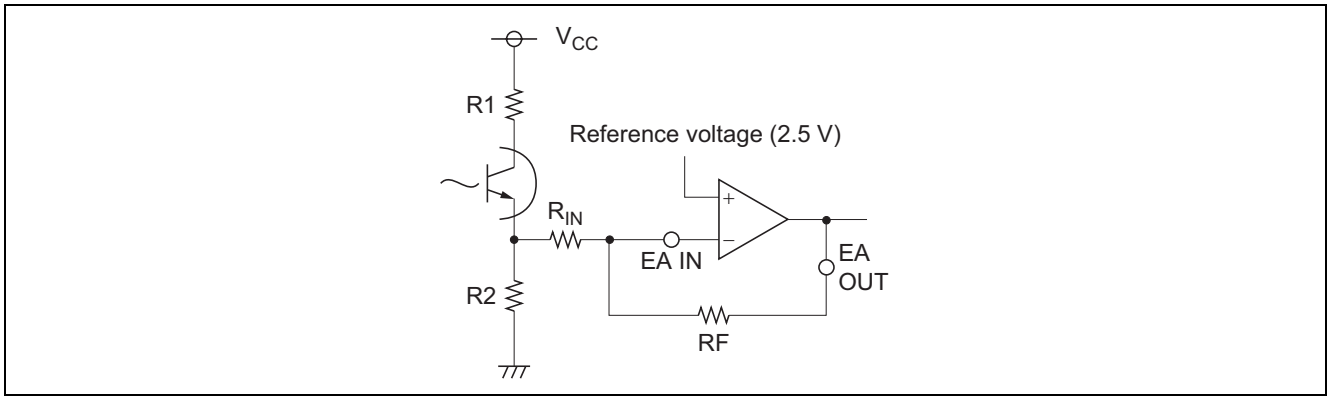


Figure 3-1 Method to Use Photo-Coupler (1)

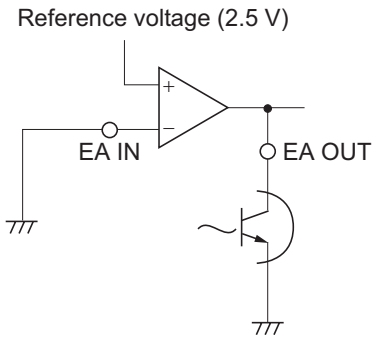


Figure 3-2 Method to Use Photo-Coupler (2)

In figure 3-1, AC gain is represented as :

$$| A_V | = | RF / R_{IN} |$$

Proper gain setting is about 40 dB.

RF should be 52 kΩ or more due to the current source capability of error amp.

R1, R2 should meet the condition as below so that the voltage of EAIN terminal should not be over 5 V.

$$R2 \bullet V_{CC} / (R1 + R2) \leq 5\ V$$

Due to the input impedance of EA IN terminal, the current in R1, R2 should be less than several mA.

CT (OVP) Terminal

Timer type latch circuit works as follows.

Constant charge current flows out from CT terminal to the external capacitor when CLM is operative.

When the voltage of CT terminal rises up to over 4.0 V (Typ.), the latch circuit operates to make functions of this IC inoperative. Inoperative status is sustained until supply voltage becomes less than stop voltage. The value for start-up register has to be set so that the current over 1.8 mA (Typ.) can flow the resistor because the stop status has to be kept by the current in start-up resistor R1 shown in application circuit.

When timer latch circuit is operative, supply current increases at high voltage as shown in figure 4 to avoid the damage caused by unnecessarily increased supply voltage.

Inoperative status goes back to operation by forcibly decreasing the voltage of CT terminal to less than 0.7 V.

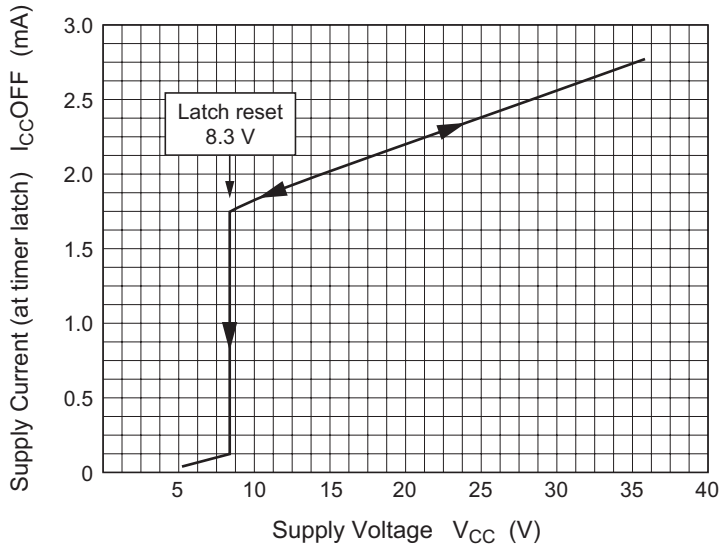


Figure 4 Supply Current vs. Supply Voltage Characteristics (at Timer Latch)

Even if the timer function is not needed, latch function operates, that is, IC becomes inoperative when the voltage of CT terminal is forced to be high voltage. Therefore, CT terminal can also be used for OVP (over voltage protection).

When only OVP function is needed (timer latch function is not necessary), connect the resistor between CT terminal and GND. In this case, the above mentioned charge current cannot make the voltage of CT terminal rise up to "H" threshold, thus latch function does not operate. (Refer to figure 5-1, 5-2)

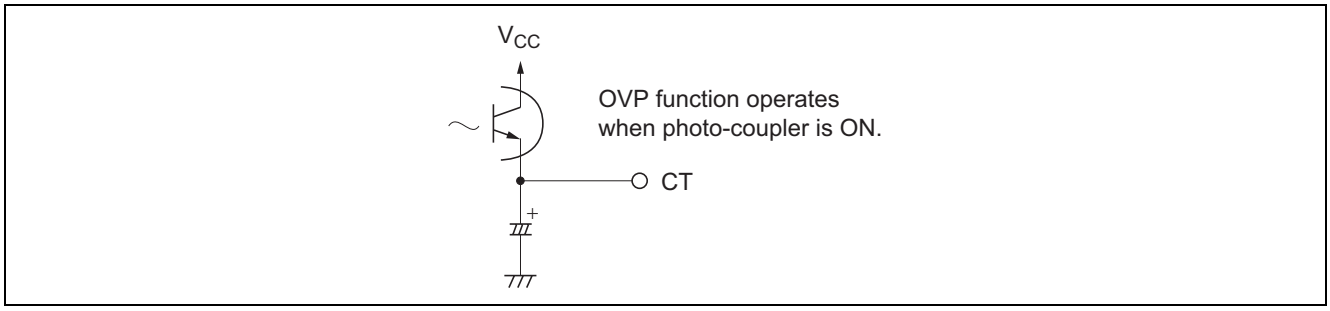


Figure 5-1 Method to Use Timer Type Latch and OVP

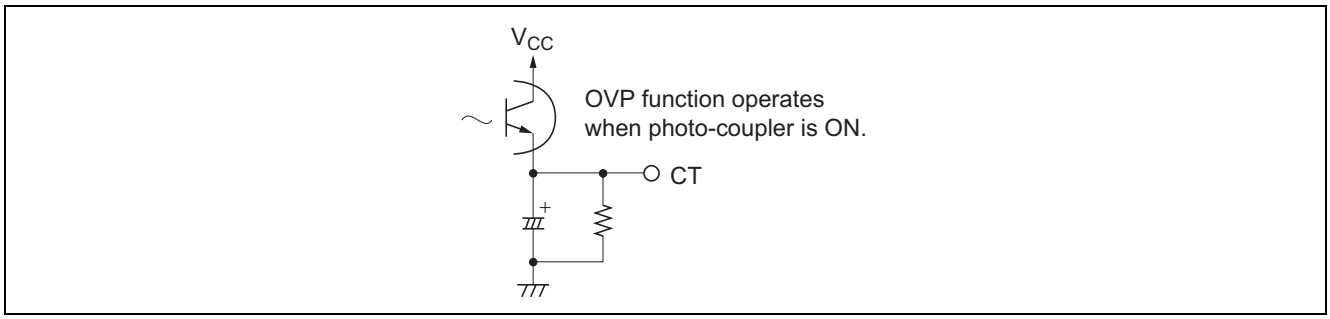


Figure 5-2 Method to Use Only OVP

SOFT(Duty Set-Up) Terminal

The voltage of SOFT terminal determines the maximum duty.

Maximum duty can be set by connecting the resistor as in figure 6 because the constant current compensated for temperature flows out of this terminal.

And by connecting the capacitor between the terminal and GND, soft start function operates. That is, we can get the gradual increase of maximum duty at start-up.

Maximum duty is represented as :

$$\text{Duty (Max.)} \approx (40.5 \bullet V_{SOFT}) - 58\%$$

where $V_{SOFT} = I_{SOFT} \bullet R_{SOFT}$ (V), $I_{SOFT} \approx 50$ µA (Typ.)

If the voltage of SOFT terminal is higher than3.53 V (Typ.) (upper limit voltage of the oscillation waveform), maximum duty is internally decided to be 90%.

Soft start time (T_{SOFT}) is represented as :

$$T_{SOFT} \approx C_{SOFT} \bullet 31 \bullet 10^3 \text{ (s)}$$

T_{SOFT} means the time from start-up until the voltage of SOFT terminal goes up to higher than 1.4 V (Typ.) (lower limit voltage of the oscillation waveform).

Discharging circuit operative before start-up at V_{CC} is internally equipped so that the soft start never fail to operate at the restart of voltage supply.

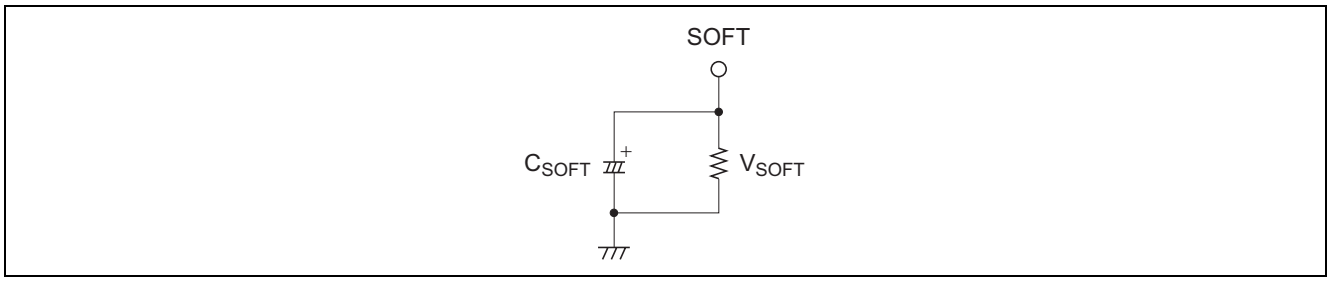


Figure 6 Method to Set-up Duty and SOFT Start Function

CLM Terminal

This terminal is for pulse-by-pulse current limiting.

Current limiting circuit is almost the same as that of M51995.

The voltage detected by the current detecting resistor can be directly input as shown in figure 7-1, if the detected voltage is about the threshold voltage (200 mV (Typ.)), but if the voltage is larger than the threshold, the voltage has to be input divided by resistors as shown in figure 7-2.

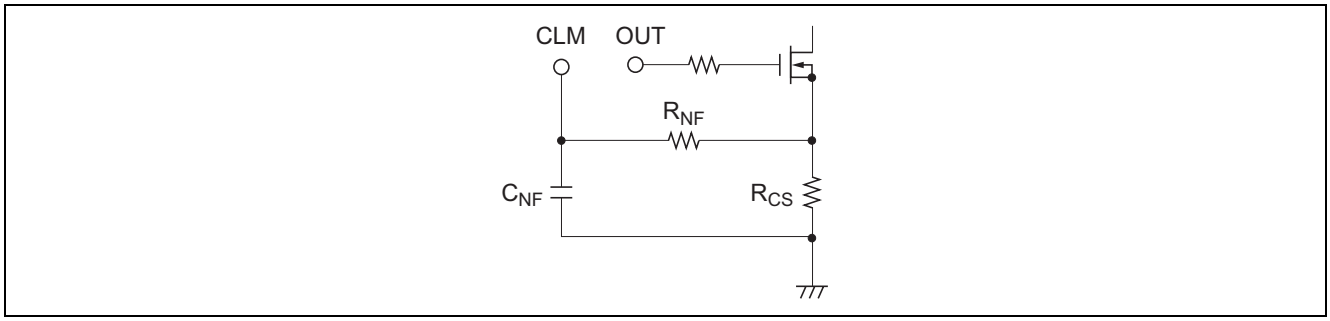


Figure 7-1 Peripheral Circuit of CLM

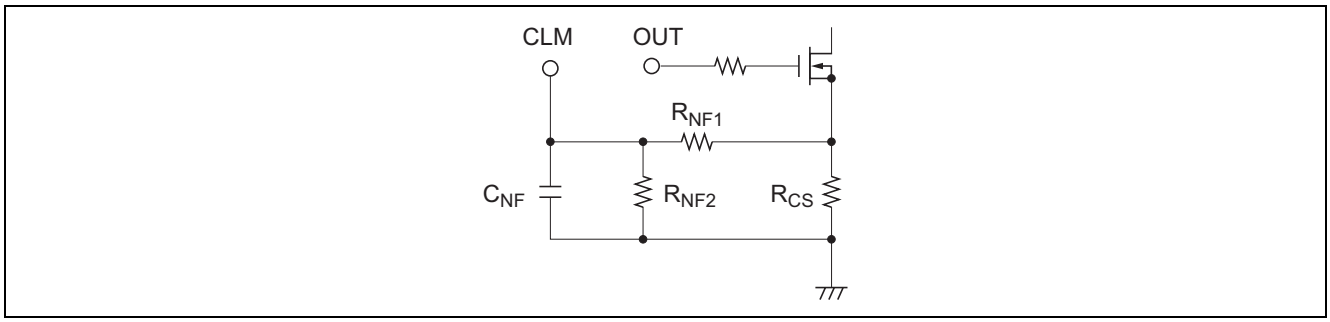


Figure 7-2 Peripheral Circuit of CLM When The Detected Voltage is High

1000 pF to 22000 pF is recommended for C_{NF}. Be sure to use 100 Ω or less for R_{NF} and R_{NF1} // R_{NF2} (*) so that the detection sensitivity is not influenced by the current flown out from CLM terminal.

Non-inductive resistor is recommended for current detecting resistor.

$$* \; R_{NF1} \,//\, R_{NF2} = (R_{NF1} \bullet R_{NF2}) \,/\, (R_{NF1} + R_{NF2})$$

Oscillation Frequency

Oscillation frequency is set by capacitor connected to CF terminal.

The waveform of CF terminal is triangular one with the ratio of 9 : 1 for charge-discharge period.

Oscillation frequency is represented as:

$$f_{OSC} \approx \frac{1}{(RF / 4.6) \bullet CF + (1.2 \times 10^{-6})} \quad (Hz)$$

Attention for heat generation

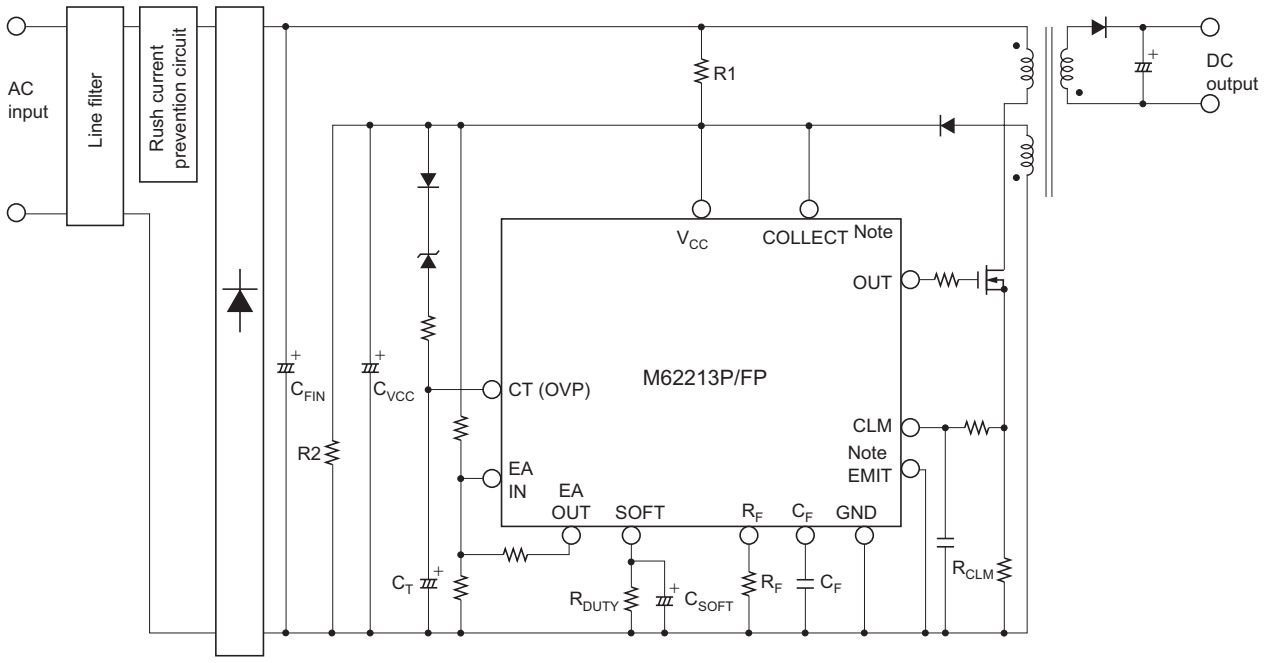
Although the absolute maximum rating of ambient temperature is spelled out as 85°C, it is always annoying to specify the location this temperature refers to because the power dissipation generated locally in switching regulator is fairly large and the temperature in the vicinity of the IC varies from place to place.

One of the recommendable ways to solve this problem is to check the temperature on the surface of the IC.

The difference in temperature between IC junction and the surface of IC package is 30°C or less when IC junction temperature is measured by utilizing the temperature characteristics of p-n junction forward voltage, and the surface temperature by "thermo-viewer" on the condition that the IC is mounted on the "phenol-base" PC board in normal atmosphere.

This concludes that maximum case temperature (surface temperature of IC package) rating is 100°C with adequate margin considering the absolute maximum rating of junction temperature is150°C.

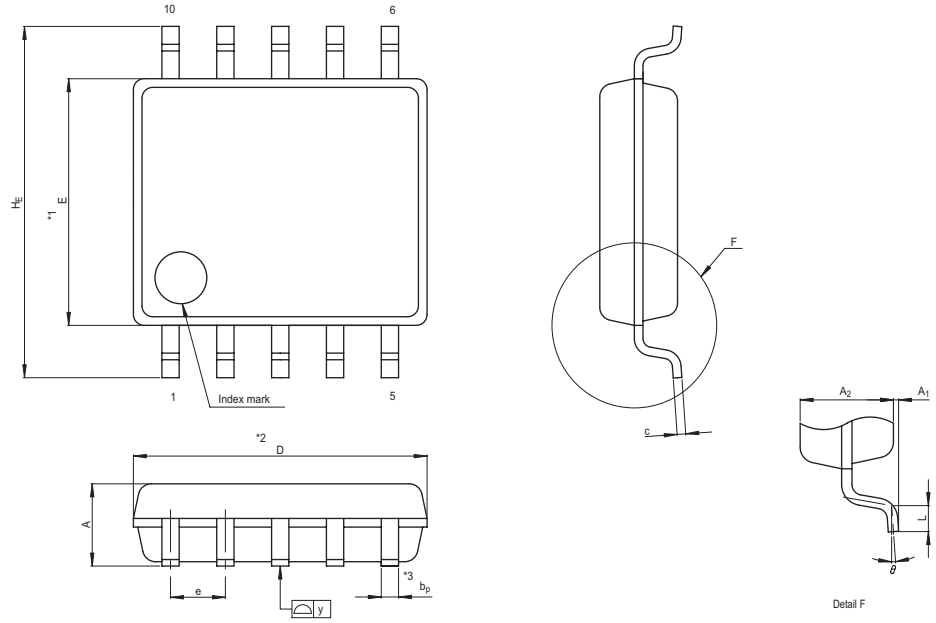
M62213 Application Circuit (Fly-Back)



Note: GND terminal is connected to emitter terminal as M62213FP in IC inside.
And V_{CC} terminal is connected to collector terminal as M62213FP in IC inside.

Package Dimensions

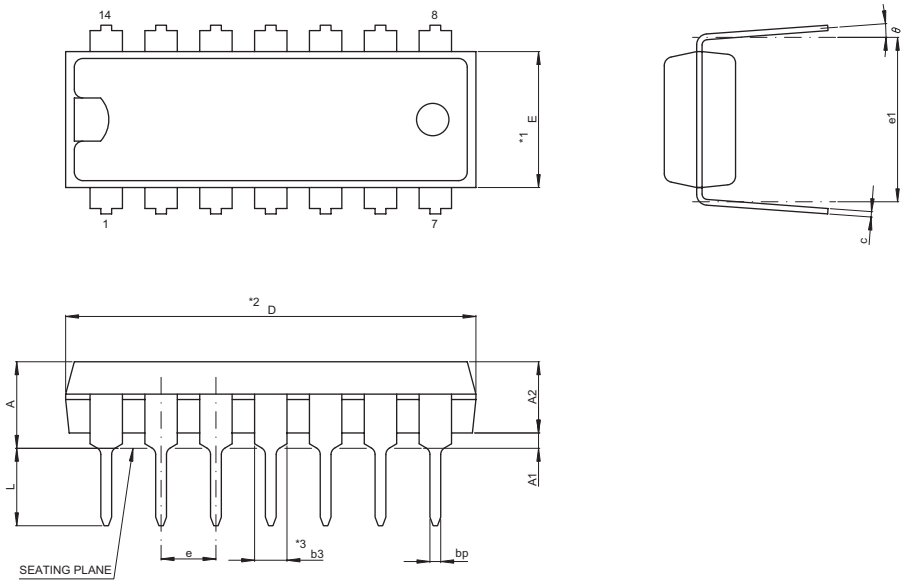
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP10-5.7x6.8-1.27	PRSP0010DB-A	10P2N-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.7	6.8	6.9
E	5.6	5.7	5.8
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.82	8.12	8.42
e	1.12	1.27	1.42
y	—	—	0.1
L	0.3	0.5	0.7

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19-2.54	PRDP0014AA-A	14P4	1.0g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

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